In the Claims:

1. (Original) A method of fabricating a thin film transistor active matrix backplane, comprising the steps of:

depositing a first passivation layer on a polyimide substrate to passivate the substrate;

applying a gate material to the first passivation layer;

patterning the gate material to form an array of gate electrodes;

depositing a gate insulating layer over the gate electrodes and the first passivation layer;

depositing a channel layer comprising amorphous silicon over the gate insulating layer;

depositing a contact layer comprising phosphorus doped amorphous silicon on the semiconducting channel layer;

depositing a source-drain layer on the contact layer;

patterning an array of source electrodes, drain electrodes, lines and pads in the source-drain layer;

patterning an array of transistor islands on the source and drain electrodes;

depositing a protective layer on the source-drain layer; and

exposing the drain electrodes and pads.

2. (Original) The method of claim 1, further comprising the step of annealing the backplane at elevated temperatures in a forming gas.

3. (Original) The method of claim 1, wherein the polyimide substrate is a flexible film.

4. (Original) The method of claim 1, further comprising the step of cleaning the polyimide substrate prior to the step of depositing the first passivation layer.

5. (Original) The method of claim 4, wherein the step of cleaning the polyimide substrate comprises the steps of:

washing the polyimide substrate; and

exposing the polyimide substrate to a plasma.

6. (Original) The method of claim 1, wherein the passivation layer comprises SiN_x.

7. (Original) The method of claim 6, wherein the step of depositing the passivation layer comprises using a gas mixture of H_2, SiH_4 and NH_3 at about 150 °C at about 0.5 Torr and about 0.067 Watts per centimeter squared.

8. (Original) The method of claim 7, wherein the passivation layer has a thickness of between about 250 nanometers and about 1000 nanometers.

9. (Original) The method of claim 1, further comprising the step of depositing a second passivation layer on a bottom surface of the polyimide substrate.

10. (Original) The method of claim 1, wherein the gate material comprises a first layer of a first metal and a second layer of a second metal overlying the first layer.

11. (Original) The method of claim 10, wherein the first metal in the gate material is aluminum and the second metal is chromium.

12. (Original) The method of claim 10, wherein the first metal in the gate material is titanium and the second metal is chromium.

13. (Original) The method of claim 10, wherein the first layer of the gate materiel is between about 500 angstroms and about 2000 angstroms thick and the second layer of the gate material is between about 50 angstroms and about 200 angstroms thick.

14. (Original) The method of claim 1, wherein the step of patterning the gate material to form an array of gate electrodes comprises providing a first mask and aligning the mask with the polyimide substrate and an array of gate electrode features and gate line features.

15. (Original) The method of claim 14, wherein the step of patterning the gate material further comprises the photolithographic steps of:

spin coating the sample with an adhesive promoter;

applying photoresist layer;

heating the sample;

etching the gate material; and

removing the photoresist.

16. (Original) The method of claim 1, wherein the step of depositing the gate insulating layer comprises using plasma enhanced chemical vapor deposition techniques.

17. (Original) The method of claim 16, wherein the gate insulating layer comprises SiN_x.

18. (Original) The method of claim 16, wherein the step of depositing the gate insulating layer uses a gas mixture of H_2, SiH_4 and NH_3 at about 150 °C at about 0.5 Torr and about 0.067 Watts per centimeter squared.

19. (Original) The method of claim 18, wherein the gate insulating layer has a thickness of between about 1800 angstroms and about 7200 angstroms.

20. (Original) The method of claim 1, wherein the step of depositing the amorphous silicon semiconducting channel layer uses a mixture of SiH_4 and H_2 at about 150 °C at about 0.5 Torr and about 0.027 Watts per centimeter squared.

21. (Original) The method of claim 20, wherein the channel layer has a thickness of between about 1000 angstroms and about 4000 angstroms.

22. (Original) The method of claim 1, wherein the step of depositing the contact layer uses a mixture of SiH_4 at about 44 sscm and PH3 at about 6 sscm at about 0.5 Torr and about 0.018 Watts per centimeter squared.

23. (Original) The method of claim 22, wherein the contact layer has a thickness of between about 250 angstroms and about 1000 angstroms.

24. (Original) The method of claim 1, wherein the source-drain layer comprises aluminum.

25. (Original) The method of claim 1, wherein the source drain layer comprises a first layer of a first metal, a second layer of a second metal overlying the first layer, and a third layer of a third metal overlying the second layer.

26. (Original) The method of claim 25, wherein the first metal in the source drain material is chromium, the second metal is aluminum and the third layer is chromium.

27. (Original) The method of claim 25, wherein the first layer of the source-drain material is about 100 angstroms thick and the second layer of the gate material is about 1000 angstroms thick and the third layer is about 100 angstroms thick.

28. (Original) The method of claim 1, wherein the step of depositing one of the source-drain and the gate metal layer comprises using one of an e-beam evaporator and a thermal evaporator.

29. (Original) The method of claim 1, wherein the step of patterning the array of source electrodes, drain electrodes, lines and pads in the source-drain layer comprises using a second mask having alignment marks and an array of source electrode features, drain electrode features, line features and pad features.

30. (Original) The method of claim 29, wherein the source-drain layer is patterned using a contact aligner.

31. (Original) The method of claim 29, wherein the step of patterning the source-drain material further comprises the photolithographic steps of:

spin coating the sample with an adhesive promoter;

applying a photoresist layer;

heating the sample;

etching the source and drain electrodes, lines and pads;

heating the sample;

dry etching the contact layer with a plasma etcher using CF_4,

removing the photoresist.

32. (Original) The method of claim 1, wherein the step of patterning the transistor islands comprises the steps of providing a third mask and using a photolithography technique to pattern the island.

33. (Original) The method of claim 32, wherein the step of patterning the channel material to form the transistor islands further comprises:

spin coating the sample with an adhesive promoter;

applying photoresist;

heating the sample;

etching the channel layer with a plasma etcher using CF_4; and

removing the photoresist.

34. (Original) The method of claim 1, wherein the step of depositing the protective layer comprises using a plasma enhanced chemical vapor deposition technique.

35. (Original) The method of claim 34, wherein the protective layer comprises SiN_x.

36. (Original) The method of claim 35, wherein the step of depositing the protective layer comprises using a gas mixture of H_2, SiH_4 and NH_3 at about 150 °C at 0.5 Torr and 0.067 Watts per centimeter squared.

37. (Original) The method of claim 36, wherein the protective layer has a thickness of about 2600 Angstroms.

38. (Original) The method of claim 36, wherein the step of patterning the protective layer further comprises:

spin coating the sample with an adhesive promoter;

applying photoresist layer;

heating the sample;

dry etching the protective with a plasma etcher using CF_4 and O_2; and

removing the photoresist.

39. (Original) The method of claim 1, wherein the step of exposing the drain electrodes and pads comprises employing a reactive ion etching technique to remove a portion of the gate insulating layer and the protective layer.

40. (Original) The method of claim 2, wherein the step of annealing has a duration of about one hour at a temperature of about 195°C and wherein the forming gas is 15 % H_2 in N_2.

41. (Original) A polymer dispersed electronic display comprising:

a backplane having an active matrix thin film transistor array formed on a flexible polyimide substrate;

a top layer of indium tin oxide coated polyester; and

a middle layer disposed between the backplane and the top layer composed of a 20:80 mixture of prepolymer PN393 and TL213;

wherein the middle layer is cured using a light source.

42. (Original) A method of making a polymer dispersed electronic display, comprising the steps of:

forming an active matrix thin film transistor array backplane on a polyimide substrate;

depositing a display medium on the active matrix thin film transistor array backplane;

depositing a protective layer comprising indium tin oxide coated polyester over the display medium; and

curing the display medium between the backplane and the protective layer.

Claim 43-95 (Cancelled).